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Nano–power-integrated precision rectifiers for implantable medical devices

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Summary

Two ultralow power CMOS full-wave precision rectifiers aimed at analog signal processing in implantable medical devices are presented. The rectifiers require no diodes and utilize a single or two transconductors (operational transconductance amplifier [OTA]) as the active element, to reduce power consumption to a minimum. First, a voltage-to-current rectifier consuming only a 120-nA supply current is presented and later is used to estimate the average AC amplitude of a piezoelectric accelerometer output (0.5–15-Hz bandwidth) in an adaptive pacemaker. This rectifier is based on a linearized transconductor and a comparator to toggle the output current sign. Then, a novel voltage rectifier consuming less than 10 nA is presented based on a single nanopower OTA and a pass transistor and later is utilized in a pacemaker's cardiac sensing channel (60–200-Hz bandwidth) circuit, incorporating the rectifier to detect positive and negative voltage signal spikes. Both rectifiers were designed in a 0.6-μm CMOS technology, fabricated, and tested, and the measurement results closely fit the expected performance.

KEYWORDS

CMOS, implantable medical devices, low power, OTA, precision rectifier

1 | INTRODUCTION

Precision rectifiers are regularly employed for analog signal processing in telecommunication, sensor, or biomedical circuits among others, to measure the average AC signal amplitude, for the detection of voltage spikes, etc. With a few exceptions, the AC component of the waveform will have any DC removed with a high (band)-pass filter or decoupling capacitor, and the voltage is then rectified utilizing one of many possible full wave precision rectifier circuits. The type of rectifier is determined by one or more requirements such as accuracy, signal frequency, or power consumption.

The overall circuit transfer of a full wave precision rectifier is

$$V_{\mathrm{Out}} = \alpha \cdot |V_{\mathrm{In}}|, \tag{1}$$

where α is a constant either positive or negative. In the case of a half wave rectifier, Equation 1 is valid only if $V_{\mathrm{In}} > 0$ (or <0). Rectifiers can be full or half wave, and equivalent current input (output) forms of Equation 1 can be defined. But in all cases, a *precision rectifier* means that the output does not depend on the voltage drop in a diode or equivalent device inside. In Figure 1A, a diode bridge rectifier is shown (it is not a precision rectifier) in comparison with a classic embodiment of a precision rectifier in Figure 1B using operational amplifiers and diodes. Unlike diode-only rectifiers

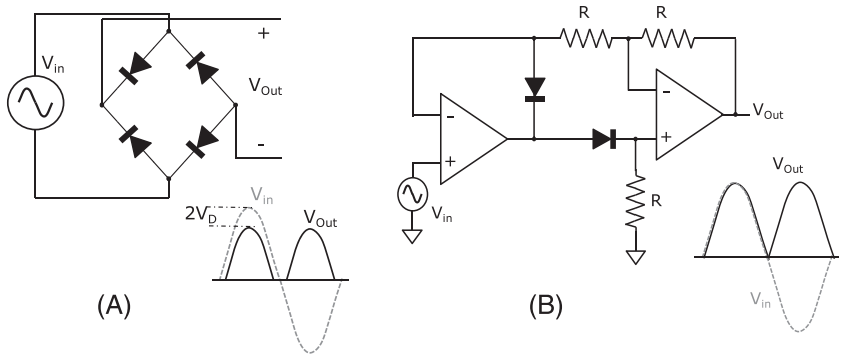

FIGURE 1 (A) A diode bridge rectifier is not a precision rectifier. (B) A classic precision rectifier circuit is based on diodes, resistors, and two operational amplifiers

like the one in Figure 1A, precision rectifiers are not aimed at extracting DC energy from an AC power supply. Instead, precision rectifiers are used to extract signal information. In the circuit in Figure 1A, there is a significant error in the output with respect to Equation 1 because of the diodes' voltage drop V_D that is not acceptable for instrumentation purposes and low amplitude signals. On the other hand, the circuit in Figure 1B is in principle ideal in the sense of Equation 1, but several other error sources may affect the output like the operational amplifiers' offset, bias current, and limited speed. Operational amplifiers also consume a relatively large supply current becoming a limit to micropower and nanopower rectifiers. In this work, the focus is on the design of ultralow power rectifiers aimed at biomedical signal processing in implantable electronics.

Biological electrical signals are not only of relatively low frequency, from quasi-DC to a few kilohertz like in electroneurograph (ENG) recording, but also of very low amplitude. Integrated precision rectifiers may help to process biological electrical signals, for example, detecting spikes of any sign as necessary in ENG or electroencephalography (EEG)[1] or measuring the average amplitude of an AC signal (just averaging the output in Equation 1) as necessary to estimate physical activity in implantable pacemakers,[2] among many other applications. Other critical aspects in the case of implantable analog circuits are minimum power consumption down to a few nanoamperes for always-on circuit blocks and an adequate accuracy while processing low amplitude signals. It should be pointed that a precision rectifier is a circuit with a nonlinearity manifesting itself at the zero-crossing, thus remains nonlinear regardless of how small the amplitude of an AC input signal is. Therefore, it is not possible to define a rectifier's offset in the sense of Equation 1, but as pointed in Arnaud and Galup-Montoro,[2] the error of the rectifier close to the zero-crossing (normally associated to an offset and limited at DC by the offset of the operational amplifiers and/or transconductors inside) is the limit to the overall biomedical analog signal processing accuracy. Also, because of the low amplitude of biomedical signals, a low-noise preamplifier and DC decoupling are normally placed before the rectifier like in Figure 2. A scheme to detect voltage spikes of previously unknown sign (could be used for ENG or EEG[1,3]) (Figure 2A) and a signal amplitude estimator (could be used for physical activity estimation (Figure 2B)[2,4]) are shown, both utilizing a precision rectifier for the task.

Finally, a general constrain to biomedical signal processing circuits is power consumption to maximize the battery life. Micropower and nanopower precision-integrated rectifiers are of special interest for implantable medical Application Specific Integrated Circuit (ASICs). But the development of such rectifiers is not trivial, firstly not only because of the power consumption of the operational amplifiers associated to classical rectifiers like the one in Figure 1B (dozens

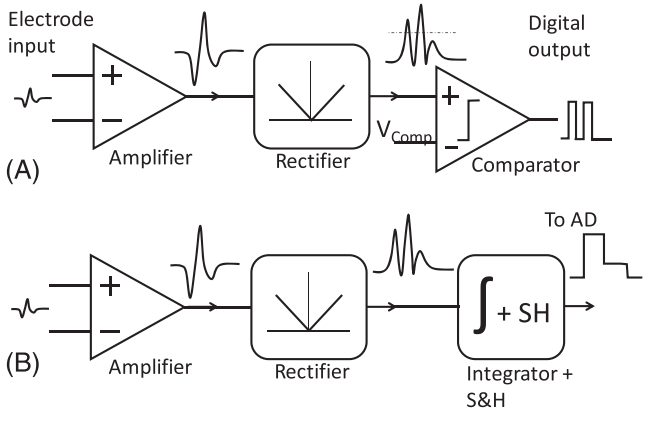

FIGURE 2 Micropower rectifiers in biomedical analog signal processing: (A) a bio-signal is amplified, and then a rectifier and a comparator are used to detect either positive or negative voltage spikes of amplitude above V_{Comp}. (B) A bio-signal is amplified; a rectifier and an integrator are used to estimate signal amplitude; an Sample&Hold samples the integration result for a CPU A/D

similar embodiments exist) but also because floating diodes are not always available in standard CMOS technology mainly due to latchup issues. The problem is challenging to such an extent that there are several published works and some patents proposing different rectifier topologies, most using either diodes and operational amplifiers, or a comparator or an equivalent structure to change an amplifier's configuration between ±1 gain depending on the sign of the input signal.[1–14]

In the present work, the development of precision CMOS-integrated rectifiers with a current consumption down to a few nanoampere and using no diodes is presented, including measurement results on fabricated CMOS-integrated circuits. First, a rectifier transconductor named G_{mRect} is shown, consuming only a 120-nA supply current. This transconductor provides at the output a current proportional to the absolute value of the input voltage. In combination with an output integrating capacitor, G_{mRect} is aimed at estimating the signal amplitude of a piezoelectric accelerometer in an adaptive pacemaker. This application operates with 0.5–15-Hz input signals in a configuration analogous to that of Figure 2B. To further reduce power consumption, a new type of rectifier is later presented requiring only a single nanopower transconductor (operational transconductance amplifier [OTA]) as the active element and consuming only a 10-nA supply current. OTA's can be realized with much less current consumption than a two-stage operational amplifier or a comparator; thus, the topology is particularly suitable for ultralow power applications. Finally, a practical complete cardiac sensing channel is presented, exploiting the latter rectifier to reduce power consumption to a minimum. In this circuit, the rectifier operates with a 60–200-Hz bandwidth input signals.

2 | A 120-NA RECTIFIER TRANSCONDUCTOR

A schematic of the proposed G_{mRect} precision rectifier is shown in Figure 3, based on a bulk-degenerated OTA.[15,16] The rectifier consists of a linearized differential pair with two different current mirrors copying the current to the output with a different sign; a second, nonlinearized symmetrical OTA G_{m2} actuating as comparator controls two NMOS switches to select which of the outputs I_{Out1} or I_{Out2} is the active one. The resulting output current is

$$I_{\mathrm{Out}} = G_{\mathrm{mRect}} \cdot |V_{\mathrm{In}+} - V_{\mathrm{In}-}|, \tag{2}$$

where G_{mRect} is the effective transconductance of the rectifying OTA and is related to the effective transconductance of the linearized input pair G_{mPair}. Using an N-series to M-parallel divider like in Figure 3, the copy factor to the output is $1/(M{\cdot}N)$[17]; thus, $G_{\mathrm{mRect}} = G_{\mathrm{mPair}}/(M{\cdot}N)$ could be as small as necessary. G_{m2} schematic is shown in Figure 4; it is a

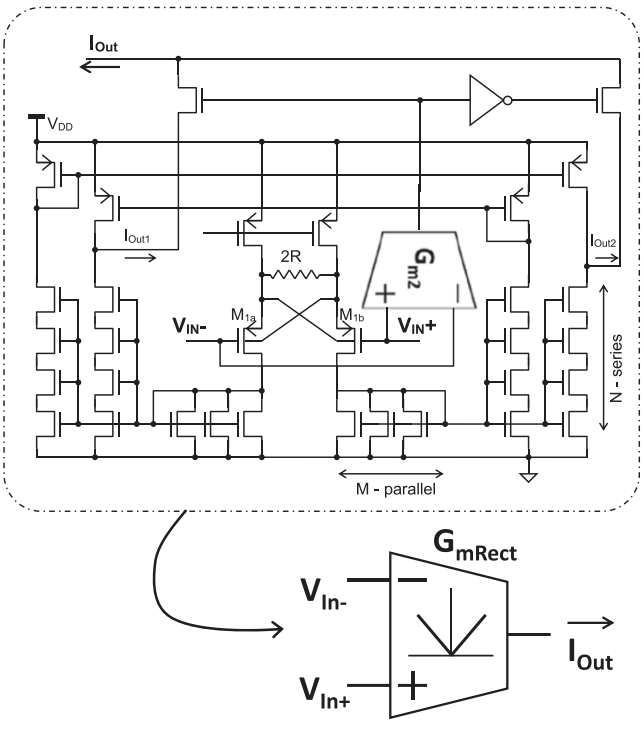

FIGURE 3 Precision voltage-to-current rectifier based on a linearized operational transconductance amplifier (OTA). The comparator G_{m2} selects which output current I_{Out1} or I_{Out2} is connected to the output; thus, the overall output current is $I_{\mathrm{Out}} = G_{\mathrm{mRect}}{\cdot}|V_{\mathrm{In+}} - V_{\mathrm{In-}}|$

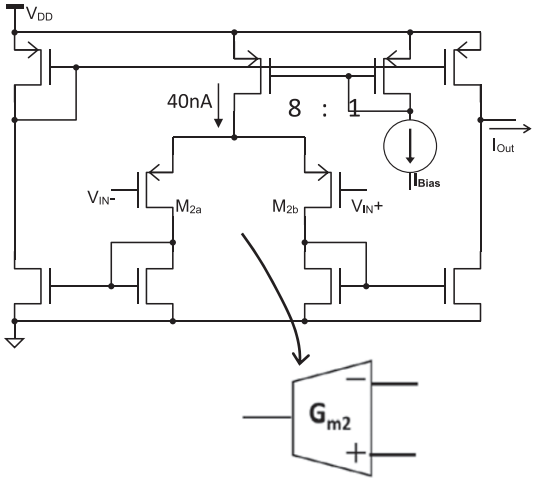

FIGURE 4 G_{m2} is a standard symmetrical operational transconductance amplifier (OTA), with wide input transistors biased in weak inversion to reduce the input offset

standard symmetrical OTA. In Figure 5, the simulated rectifier output is shown, for an effective pair's transconductance $G_{mPair} = 160$ nS corresponding to the case $2{\cdot}R = 7.5$ MΩ, $(W/L)_1 = 48$ μm/12 μm, the bias current of each transistor in the pair of Figure 3 $I_1 = 40$ nA, and $M = 8$, $N = 4$, the resulting $G_{mRect} \approx 5$nS. The combined bulk and source degeneration technique was employed to maximize the input range, but it is also possible to use source degeneration only like in Arnaud and Galup-Montoro and Krummenacher and Joehl.[2,18]

The advantages of the proposed rectifier are as follows:

1 Firstly is the minimum power consumption because the comparator is just a nanopower OTA connected to a minimum capacitive load; no operational amplifiers are used to set a virtual ground.
2 Secondly is the DC precision as the offset of the OTAs can be limited to a couple of millivolts for an untrimmed circuit.[2,17]

A G_{mRect}C amplitude estimator can be implemented like in Figure 6, just by connecting an R_1–C_1 network at the output of the rectifier. This circuit is employed in the configuration of Figure 2B to estimate the physical activity of the patient with an adaptive pacemaker. The output of a piezoelectric accelerometer is amplified and filtered ($G = 50$ dB, bandpass of 0.5–15 Hz), and then the average amplitude in the last 5 s is estimated with the circuit in Figure 6, and the pacemaker's CPU samples, converts, and processes this value at a very low rate to save power.

The circuit was fabricated in a 0.6-μm CMOS technology with high-voltage (HV) capabilities and measured. Although the circuits in this work use exclusively low-voltage transistors, the HV technology was selected because it provides also native HV transistors (up to 45 V V_{DS}) as necessary in the tissue stimuli section of many implantable circuits. The low-voltage transistors have a relatively large threshold voltage $V_{TN} \approx \square\ V_{TP}\ \square \approx 1$ V which limits the minimum supply voltage to 1.5 V, but the large V_T also helps to reduce leakages to a negligible value as necessary in nanopower applications. The circuit properly operated for a 1.5 V < V_{DD} < 5.5 V supply voltage, which is compliant with most medical grade batteries; pacemakers for example are normally powered by a primary lithium iodine cell

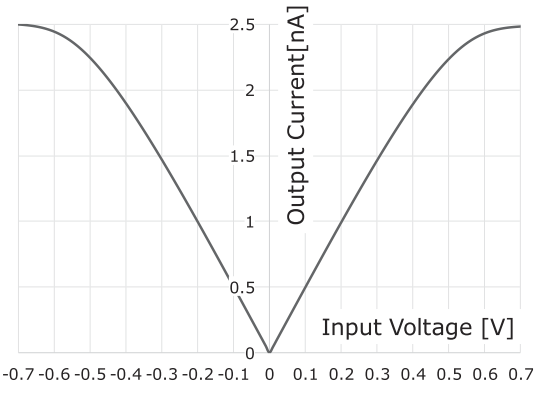

FIGURE 5 Simulated voltage-to-current precision rectifier output, for an effective pair's transconductance $G_{mPair} = 160$ nS, $M = 8$, $N = 4$, resulting in a rectified output current to input voltage ratio $G_{mRect} \approx 5$ nS

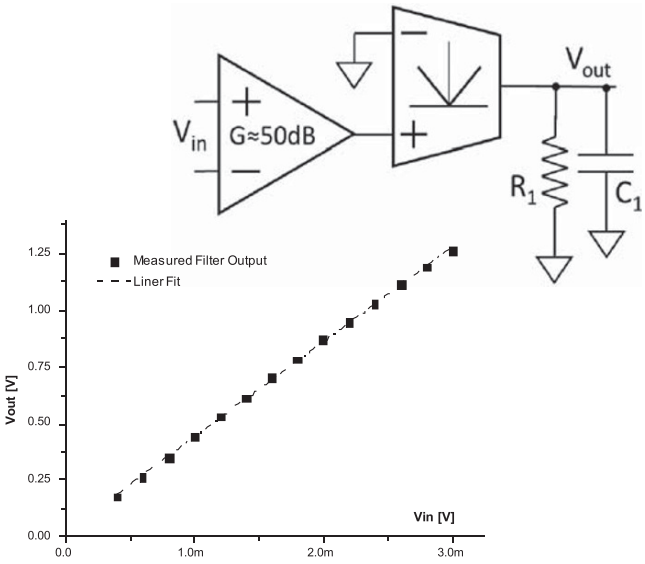

FIGURE 6 Measured linearity of an amplifier and G_{mRect}C amplitude estimator using the developed rectifier, while varying a 5-Hz sinusoidal test input amplitude. Measured values (squares) and a linear regression (dash-dot line) are shown; the correlation coefficient is $r > 0.99$. $R_1 \cdot C_1$ time constant is 5 s

ranging from 2.8 to 2.0 V (beginning to end of battery life), and always-on circuit blocks are directly connected to it. A microphotograph of the rectifier is shown in Figure 7. Measured results are shown in Figure 6 for the amplitude estimator based on G_{mRect}, using an external resistor $R_1 = 10$ MΩ and capacitor $C_1 = 470$ nF, connected at the output resulting in a $R_1 \cdot C_1 \approx 5$ s time constant. The scheme is analogous to that of Figure 2B, but the output is a continuous time signal. The total power consumption of the rectifier is 120 nA (80 nA for the input pair and 40 nA for G_{m2}), and the estimated input pairs' offset standard deviation, which can be associated to the amplitude estimator precision, is only $\sigma_{\mathrm{offRect1}} = 4$ mV. In the case of G_{m2}, its input offset is much lower $\sigma_{\mathrm{offGm2}} < 1$ mV because the input transistors are biased in weak inversion (WI) and are nonlinearized. In the case of the physical activity estimation circuit, an equivalent 5-$\mathrm{mV_p}$ to 5-Hz input in the rectifier was properly detected by the CPU AD, which can be associated to the minimum rectifier's input signal.

3 | A NOVEL 10 NA PRECISION RECTIFIER

Although the rectifier in Figure 3 is adequate for implantable electronics, it still consumes some power due to the necessary current to linearize the input differential pair (80 nA even in the case of the small G_{mRect} of Figure 3) and the current consumption of G_{m2} OTA (40 nA) necessary to toggle the output transistors relatively fast. To further reduce the power consumption to a negligible value, a new rectifier is proposed in Figure 8. It is composed of a transconductance amplifier G_{m}, a single NMOS pass transistor M_1 and two identical resistors R_1 and R_2. The negative input $e-$ of the OTA is connected to a reference voltage V_{Ref} that is the analog signal ground. The rectifier can be analyzed separating two cases depending on the input signal V_{In}, which is above or below V_{Ref}. In the first case, the OTA will control

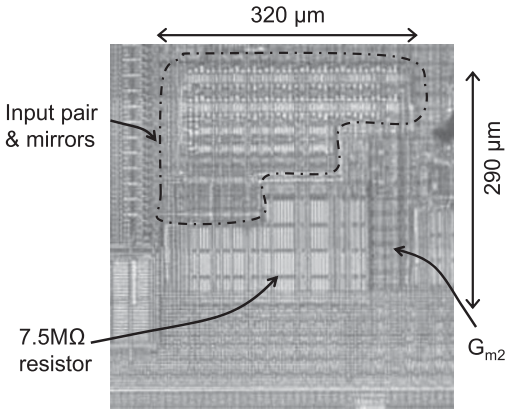

FIGURE 7 Microphotograph of G_{mRect} occupying a 290 × 320-μm^2 die area

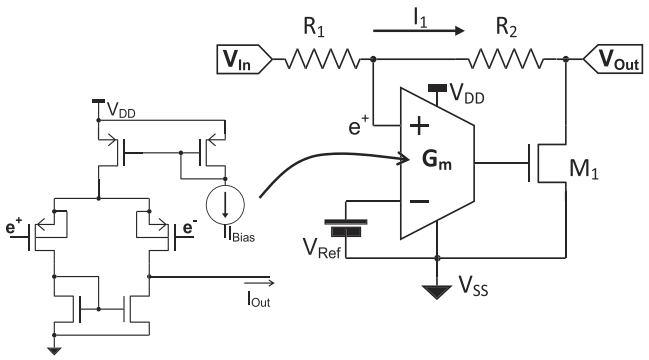

FIGURE 8 Schematic of the proposed 10-nA feedback rectifier

the M_1 gate to establish a feedback (FB) loop, making the node $e+$ of Figure 8 almost equal to V_{Ref}. Because of this reason, we will denote it as a FB rectifier. The loop is possible because the gate to source voltage V_{GS1} of M_1 rises, allowing a positive current I_1 to flow through R_1–R_2–M_1. Because $R_1 = R_2$, the voltage drops are equal with respect to V_{Ref} thus, the output voltage $V_{\text{Out}} = -V_{\text{In}}$ and the circuit behaves as a (−1) gain amplifier. In the second case, when V_{In} is below V_{Ref}, the OTA will first discharge the gate of M_1, but a FB loop is not possible because a negative I_1 cannot flow in steady state. The transistor M_1 is in this case cut off; therefore, considering an infinite output load, there is no voltage drop through $R_1 - R_2$, and V_{Out} is equal to V_{In}. The overall circuit transfer is that of a precision rectifier:

$$V_{\text{Out}} = -|V_{\text{In}}|. \tag{3}$$

It should be highlighted that when $V_{\text{In}} > V_{\text{Ref}}$, the FB loop is established regardless of whether the transistor M_1 is in weak, moderate, or strong inversion or even in the linear zone behaving as a resistor; the situation is analogous to the active current mirrors presented in Miguez et al.[19] where the circuit theory is discussed in detail. When $V_{\text{In}} < V_{\text{Ref}}$ instead, a FB loop is not possible because G_{m} cannot set V_{GS1} to a point where $I_1 < 0$. I_1 can be negative only for a very short period while any parasitic output capacitance is discharged, and V_{GS1} lowers until V_{GS1} 0 when the transconductor in no more linear and I_{Out} in Figure 8 is null even though $e+ < e-$.

The main advantages of this rectifier are its simplicity and the very low current consumption because the OTA bias current can be as low as a few nanoamperes depending on the required rectifier speed. In the presence of a large input signal, the current through the resistive divider should be also considered for current consumption estimation. On the downsides, the rectifier behavior is affected by the output load especially when $V_{\text{In}} < V_{\text{Ref}}$, and the designer must take care of the loop stability when $V_{\text{In}} > V_{\text{Ref}}$. The accuracy of the rectifier is limited by the OTA's input referred offset and R_1–R_2 matching.

The rectifier design was oriented to minimum current consumption, as it is aimed at being part of a signal amplitude estimation block in an implantable medical device. The OTA G_{m} of Figure 8 is a differential pair with an active load, biased with $I_{\text{Bias}} = 8$ nA only. Both the differential pair and lower current mirror are biased in WI, the resulting transconductance is $G_{\text{m}} = 120$ nS. The estimated input referred offset standard deviation of the transconductor is $\sigma_{\text{offGm}} \approx 1.7$ mV. R_1 and R_2 are two matched $R_1 = R_2 = 10$ MΩ resistors implemented with high resistivity poly, and M_1 is a $(W/L)_1 = 40$ μm/2 μm transistor. A MOS-input buffer with a 2-pF input gate capacitance was connected at the rectifier's output for test purposes. The rectifier can operate with a supply voltage V_{DD} in a very wide range from 1.5 to 5.5 V.

In Figure 9, the simulated response of the rectifier is shown, for both a small 10-mV and a larger 100-mV 100-Hz sine wave inputs. Note the distortion in the zero-crossings at time = 10 or 20 ms (increasing V_{In}) because it takes some time to turn M_1 on again to set the FB loop. Also, at time = 5, 15, and 25 ms (decreasing V_{In} zero crossings), $V_{\text{out}} < 0$ because it also takes some time to completely discharge the M_1 gate. Both effects can also be observed in the measured plots of Figure 10. Distortion can be reduced just by increasing the OTA's bias current, making possible to faster charge/discharge the M_1 gate in the transitions.

In Figure 10, the measured response of the rectifier of Figure 8 is shown, for a large 420-mV_p sine wave at the input, a ±200-mV_p dual pulse CENELEC signal (it is a standard triangle pulse with 2 ms rise and 13 ms fall times[20]), and a 50-mV sine wave input signal.

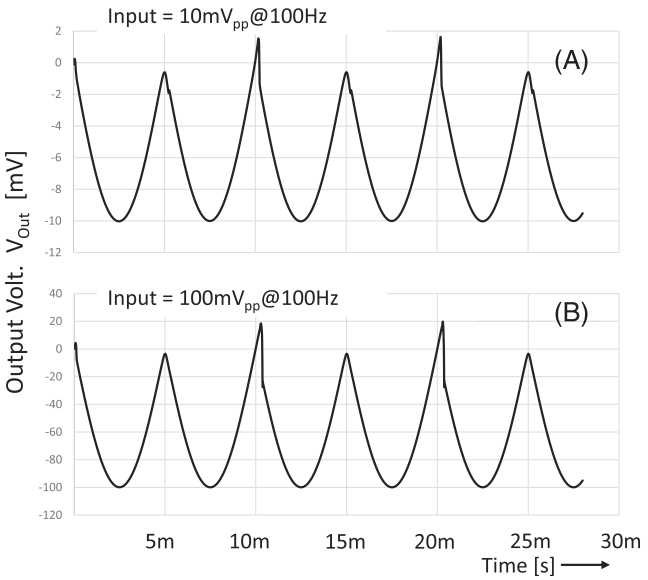

FIGURE 9 Simulated output plots for (A) a small 10-mV sine wave input, (B) a larger 100-mV sine wave input. The waves are referenced to $V_{\text{Ref}} = 0.8$ V, $V_{\text{DD}} = 2.8$ V

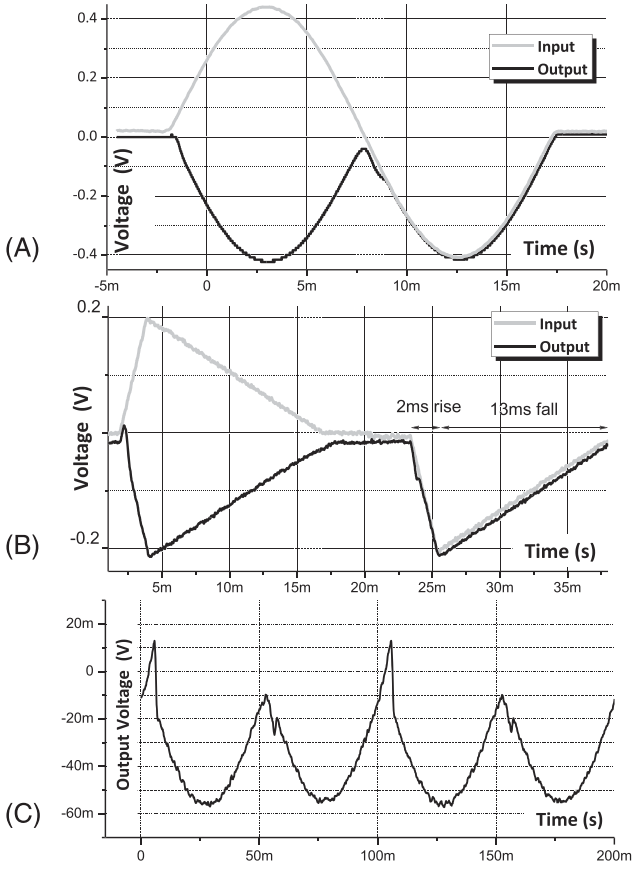

FIGURE 10 Measured integrated rectifier input–output plots for (A) a large 420-mV sine pulse, (B) a CENELEC test wave,[20] (C) output only for a 50-mV$_p$ small amplitude sine wave input. $V_{\text{Ref}} = 1.2$ V, $V_{\text{DD}} = 2.8$ V, $V_{\text{SS}} = 0$ V in all cases. A 2-pF load buffer is connected at the output

4 | A PRACTICAL BIOMEDICAL CIRCUIT APPLICATION

A complete pacemaker cardiac sensing channel[20–22] is shown in Figure 11, as an application example for the developed nanopower precision rectifier. The circuit is aimed at pacemakers to detect the heart's natural electrical activity. The objective is to generate a digital output when signal spikes higher than a programmable amplitude are present at the input. The input signal is amplified (peak gain is ×170) and filtered between approximately 60–200 Hz[21] by the integrated differential input amplifier of Figure 11 (it is similar to the preamplifier in Lentola et al.[22]) and then connected

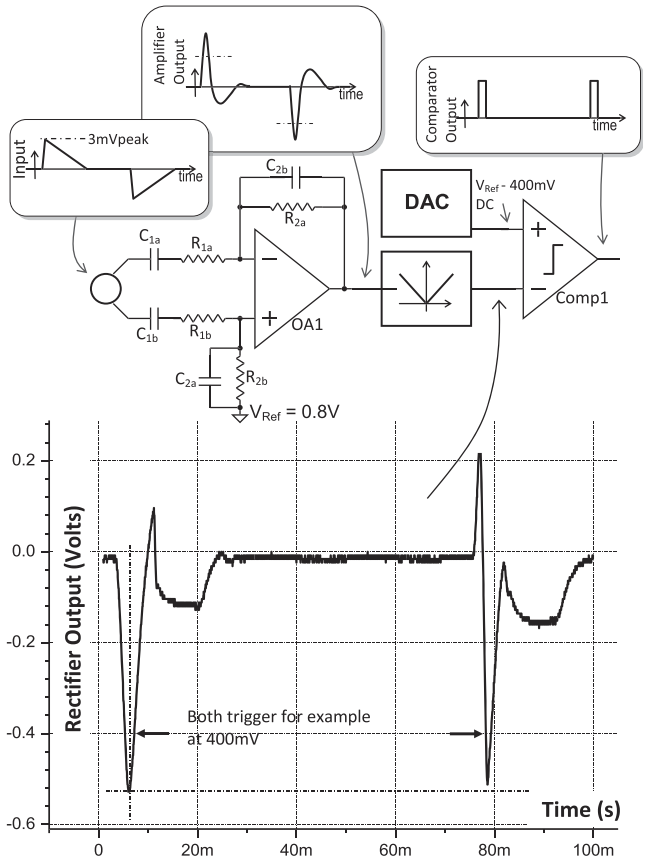

FIGURE 11 The fabricated complete cardiac sensing channel and the measured output of the rectifier, when a standard positive–negative 3-mV_p CENELEC wave test signal is applied at the input

through the rectifier to a programmable threshold comparator that provides a digital pulse at the output each time the amplified signal surpasses the output V_{Comp} of a 6-bit DAC. The standard test signal to simulate the cardiac natural electrical activity is a 200-μV_p to 8-mV_p single triangle pulse like the ones in Figure 10B (usually denoted as CENELEC test signal[20]). Most pacemakers are specified to detect both positive and negative spikes using, for example, a second comparator like in Prutchi and Norris,[21] but a more power-efficient solution is to place a precision rectifier before a single comparator like in Figure 11. The resulting scheme is analogous to that of Figure 2A. The complete circuit of Figure 11 was integrated in the same 0.6-μm technology; only the 33-nF input capacitors, C_{1a} and C_{1b}, are external because of their size but also for safety issues in a real pacemaker. A measured rectified output, corresponding to a 3-mV_p CENELEC input is shown on the bottom of Figure 11.

In Figure 12, the schematic of the comparator in Figure 11 is shown. It is a symmetrical OTA with a $(W/L)_1 = 100\mu m/6\ \mu m$ input pair biased in WI and an inverter chain at the output. These large input transistors are used to reduce mismatch offset, and the M_{1a} and M_{1b} bulks were deliberately connected to V_{DD} to increase the gate-source voltage V_{GS1} to guarantee the input common mode range goes down to V_{SS}. The bias current $I_{Bias} = 50$ nA, and the *Sel* signal in Figure 12 is used to turn the comparator on/off through the small M_{S1} and M_{S2} transistors to avoid unnecessary current consumption when not in use. The operational amplifier in Figure 11 is a standard two-stage Miller compensated amplifier with NMOS input transistors sized 100μm/6 μm to preserve a reduced input offset, and on/off capability sharing the *Sel* signal with the comparator. In Figure 13, a microphotograph of the circuit in Figure 11 is shown (OA1, Comp1, Rectifier). In the case of the rectifier, the occupied area is 250 μm × 400 μm, corresponding mostly to the resistors.

In Figure 11, the comparator's input was estimated to represent a 2-pF MOS capacitor load for the rectifier that in a first approximation does not affect its operation. While the rectifier output of Figures 10 and 11 is not perfectly symmetrical, the input referred detection error of the sensing channel is below 100 μV for a positive/negative spike, which is adequate for the pacemaker application according to European Standard.[20] The origin of the asymmetry is the relatively high speed of the large rectified signal and can be corrected by reducing R_1 and R_2 values (R_1 and R_2 in the tens of MΩ range are not strictly necessary) or with an increase in the bias current of the FB OTA G_m. It should be pointed that the operational amplifier OA1 and comparator Comp1 in Figure 11 joint current consumption is close to 800 nA, which is

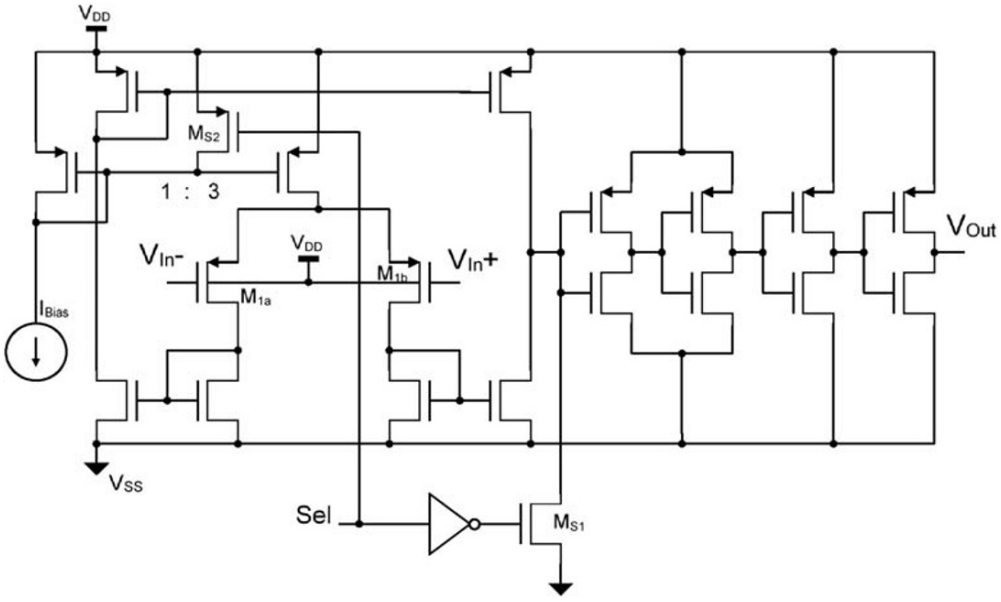

FIGURE 12 Comp1 comparator schematic; the *Sel* signal turns the comparator on/off to avoid unnecessary current consumption when it is not used

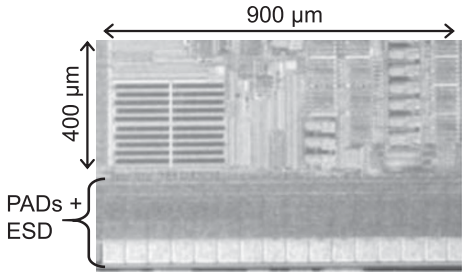

FIGURE 13 Microphotograph of the integrated cardiac sensing channel, contact padss, and Electrostatic discharge (ESD) protections at the bottom

also consistent with the values presented in Lentola et al.[22]; thus, a much large current budget can be assigned to the rectifier.

4.1 | Linearity, precision, and maximum frequency considerations

In the case of a precision rectifier aimed at extracting signal information in a biomedical signal processing circuit, it is important to know the minimum and maximum input amplitude and the maximum input frequency it can process. Also, although a rectifier is a nonlinear circuit, it is important that the output amplitude is proportional to the input amplitude. In Figure 14, the measured output peak amplitude for the circuit in Figure 8 when the input is a 100-Hz sine

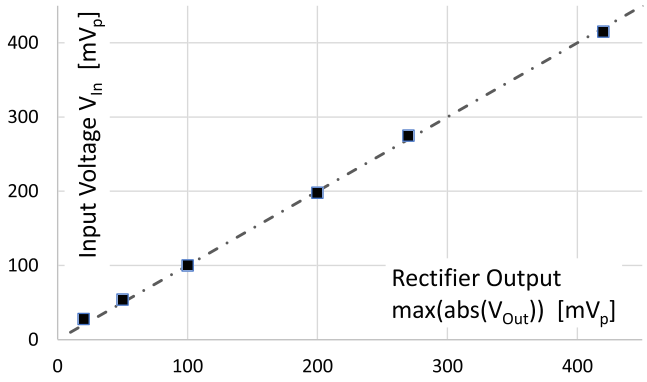

FIGURE 14 Measured rectifier peak output, for different sine wave inputs showing the linearity of the proposed rectifier-based peak detector. The dash-dot line corresponds to the simulated values [Colour figure can be viewed at wileyonlinelibrary.com]

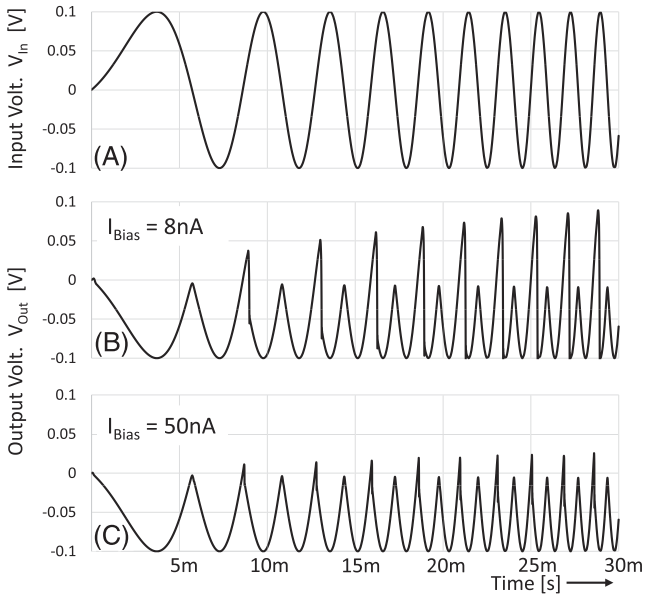

FIGURE 15 Simulated rectifier output for a 100-mV_p amplitude variable frequency sine wave input. (A) Input voltage, (B) rectifier output operational transconductance amplifier (OTA) I_{Bias} = 8 nA, and (C) rectifier output OTA I_{Bias} = 50 nA, Note the zero-crossing distortion increases with frequency because of the faster input transition

wave is presented, showing a good linear response as expected from the simulations in the same plot. The maximum frequency cannot be easily defined in this case because the problem is not the attenuation of the output like in a linear circuit but the distortion of the signal as the frequency increases. In Figure 15B, the simulated rectifier output is shown for a variable frequency sine wave input. Note the zero-crossing distortion increases with frequency because of the faster input transition. The problem is not so important in the case of the cardiac sensing channel of Figure 11 because the negative peak to detect is not affected. In Figure 15C, the same simulation is presented, but the bias current of G_m was increased to 50 nA, allowing the FB loop to better track the changes in the input so the distortion is greatly reduced. Thus, for the proposed rectifier, the maximum operating frequency for a given acceptable distortion can be enhanced just by assigning an extra current budget to the OTA. The OTA was finally designed with just an 8-nA bias current because the maximum frequency to consider for cardiac signal detection is □200 Hz,[21] but also as a proof of concept to demonstrate a minimum power rectifier in a practical application.

The minimum signal the rectifier can process is in the order of the G_m OTA offset which was estimated as 1.7 mV; also, the system in Figure 11 was measured, and it properly detected a small positive/negative CENELC input wave corresponding to 5-mV amplitude at the rectifier's input. Finally, another advantage of the rectifier in Figure 8 is that because the transconductor operates at small differential input voltages ($\underline{e}+ - e-$) and the resistors are linear regardless of the applied voltage, the maximum input signal to rectify can be very large and close to V_{DD}.

TABLE 1 Comparison of the proposed rectifiers

	This work 120-nA G_{mRect}	**This work 10-nA FB rectifir**	**[23]**	**[10]**	**[14]**	**[13]**
Technology	0.6 µm	0.6 µm	180 nm	0.35 µm	0.35 µm	180 nm
Supply voltage (V)	1.5–5	1.5–5	0.6	1	1	1.2
Current consumption (nA)	120	10	□3500	60	5200	1000
Max. input amplitude (mV_p)	550	1700[a]	250	230	450	850
Max. frequency (Hz)	>200[c]	200[d]	200 k	100	30 k	20 k
Circuit área (mm^2)	0.093	0.10[b]			.057	□0.035

Abbreviation: FB, feedback.
[a]@V_{DD} = 3.7 V, V_{Ref} = 2 V can be larger/lower depending on V_{DD} and V_{Ref}.
[b]Area corresponds almost exclusively to the large poly resistors.
[c]The rectifier was tested up to 200 Hz without a significant amplitude attenuation.
[d]Application maximum frequency

5 | CONCLUSIONS

Two ultralow power CMOS full-wave precision rectifiers requiring no diodes were presented. The first is a full-wave voltage-to-current rectifier consuming only 120 nA; it was designed, fabricated in a 0.6-μm technology, and tested. The rectifier was used in a nanopower amplitude estimator for the output signal of a piezoelectric accelerometer exhibiting a very good linearity. To further reduce power consumption, a novel full-wave precision voltage rectifier topology was developed, and a nanopower rectifier consuming less than 10 nA was designed, fabricated in the same CMOS technology, and measured. In Table 1, some characteristics of the rectifiers are presented together with other reported low power precision rectifiers. The proposed rectifiers consume very little current and can process very large input signals, exhibiting a good measured linearity. The maximum input frequency is low but adequate for the proposed applications. Both rectifiers were tested down to a 5-mV input signal and between 1.5- and 5-V supply voltages.

The 10-nA FB rectifier was later utilized in a cardiac sensing channel circuit for pacemakers, incorporating the rectifier to detect positive and negative voltage spikes with a negligible power consumption overhead. Measurement results closely fit the expected performance of the rectifiers and analog signal processing circuits.

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